Dual Channel Control with DC Fault Ride Through for MMC-based, Isolated DC/DC Converter

Dragan Jovcic, *senior member IEEE*, and Huibin Zhang
School of Engineering
University of Aberdeen
Aberdeen, UK

***Abstract*— This paper presents the two-channel controller with inner current loops for dual bridge, DC/DC converter, based on MMC (Modular Multilevel Converter) technology. The DC/DC control strategy is based on two inner fast current control loops in *dq* rotating frame at each of the two MMC bridges. These current controls facilitate operation through DC faults at either DC bus. The active power control is shared by two MMCs, at the slower outer control level. The second outer control loop minimizes losses, which is achieved by feedback control of magnitude of both modulation indices at maximal value of *0.95* at all loading levels. The controller is symmetrical, provides bidirectional power flow and responds equally to faults on either DC bus. Under DC fault conditions, one MMC actively controls the inner AC current, while temporary blocking of MMC on faulted side is required to prevent cell capacitor discharge. The validity of the proposed control is verified on PSCAD using a *600MW, 500kV/640kV* test DC/DC model. The controller can be used for control/stability studies with large DC grids that contain DC/DC converters.**

Keywords— HVDC transmission, DC-DC power converters, Modular multilevel converter, Average value model, DC Power Transmission

I. INTRODUCTION

The future DC transmission grids will require DC/DC converters primarily to interconnect local DC systems operating at different voltages [1]. Also DC/DC converters facilitate other functions like DC fault isolation and power flow control which makes them essential building blocks in DC grids. Two DC/DC converters are included in the CIGRE DC Grid test system [2], and they are discussed as enabling technologies in the CIGRE DC grid feasibility brochure [3].

There has been lot of research on high voltage DC/DC converter topologies and the transformerless concepts [4]-[6] have demonstrated numerous technical advantages. The single-arm concepts, and poliphase cascaded cell DC/DC offer potentially optimal semiconductor count, but current sharing is unequal (facilitating only low stepping ratio), there is no isolation and DC fault blocking is only achieved if full-bridge cells are employed. The LCL DC/DC concept [6] uses DAB (Dual-Active-Bridge), enabling high stepping ratio and good DC fault ride through, but galvanic isolation is not achieved.

Galvanic isolation requires an inner medium-frequency transformer with associated cost/weight/size drawbacks, but offers flexibility in grounding, better safety under contingencies and it seems to be preferred choice in industry [7]. Considering also technology readiness, modularity and standardization, it is likely that manufacturers will firstly choose transformer-isolated DC/DC employing two DC/AC bridges based on MMC (Modular Multilevel Converter) technology [7][8]. MMC approach has higher voltage capability, low harmonics, low losses and modularity. In order to reduce size with acceptable losses, the operating frequency can be adopted in the range *300-500Hz* [8][9]. The MMC converters are nowadays well developed for *50Hz* grid connections and it is not expected that significant difficulties will arise if operating frequency is elevated to *350Hz* [9].

The design of high-power isolated DAB DC/DC converters has attracted lot of research in recent years [10]-[16]. Many advances have been made in design of inner MMC, such as loss reduction using softswitching techniques in quasi-square-wave modulation [10], improved cell voltage balancing control [11], or reducing computation burden caused by balancing and modulation of large number of cells [12]. A medium frequency (1kHz), 1kW prototype, with 4 cells in an arm and stepping ratio of 3, isolated DC/DC is demonstrated in [13]. The power is controlled using phase shift between two AC voltages and it is recognized that DC/DC can be used as DC CB (Circuit Breaker) by blocking both MMC. Reference [14] gives thorough comparison of design and losses of 3 variants of DAB concept. In [15] three modulation methods for MMC are compared and it is recognized that *sine* modulation has lowest circulating (reactive) power which reduces conduction losses. The overall efficiency on a 2kW, 2kHz DC/DC prototype in [15] was highest with square wave modulation, but *sine* wave modulation with nearest level control may be more suitable with GW–size converters because of switching losses and limits on harmonics [8][9].

The above references do not analyse DC/DC operation under DC fault conditions, which is nevertheless very important for HVDC applications. DC faults are simulated in [16] but similarly as in [13] it is recommended that both DAB bridges are blocked for a DC fault on either side. However, blocking whole DAB DC/DC requires long restart time, which is a particular disadvantage for transient DC faults. If DC/DC is embedded in a large DC grid with many DC lines and many DC CB (Circuit Breakers), then most faults will be seen as transient. A DC fault may depress DC voltage on many DC busses for around 5-30ms while it is being cleared by DC CBs. It is desired that DC/DC operates through DC faults on

This study is sponsored by the Engineering and Physical Sciences Research Council (EPSRC) grant no EP/K006428/1, 2013.D. Jovcic and H. Zhang are with the School of Engineering, University of Aberdeen, AB24 3UE, U.K. (d.jovcic@abdn.ac.uk, huibin.zhang@abdn.ac.uk).

other DC lines in order to enable fast DC grid recovery and to retain control on the healthy DC bus.

During DC faults it is also desired to facilitate current control, because of small thermal constants of semiconductors. Inner current control is well developed for 50Hz MMC converters but two MMC in a DAB share the same current which brings challenge of coordination between bridges.

Typically DC/DC studies use quite simple control, based on one control channel (phase shift) for power flow regulation [10]-[16], and MMC blocking for DC faults [13],[16].

This study aims developing a comprehensive controller for DAB MMC DC/DC that permanently utilizes inner current control loops, enables operation for worst case DC faults and minimizes current at any loading. The study will aid in understanding dynamics, capabilities, operating modes and boundaries of high power DC/DC and its integration with HVDC. The findings will be of use in studying large DC grids with multiple DC/DC, DC grid power flow, DC grid control, dispatching and dynamics, as in the test systems in [2][3].

II. DC/DC CONVERTER PHASOR MODEL

A. DC/DC Converter Topology

The schematic of DAB MMC isolated DC/DC converter is shown in Figure 1. It consists of two AC/DC converters MMC1, MMC2, a power transformer *Tr*, and a series inductor per phase L_{ac} which is required to limit fault current peaks. In general a DC/DC can have 2 or more phases depending on power level and rating of selected IGBTs [9],[13]. The study below equally applies to any number of phases, assuming that proper *dq* transformation is used.

Figure 2 shows per-phase equivalent inner AC circuit. The subscripts 1,2 indicate variables of different MMC. The following parameter relations exist:

$$R'_2=R_{tr}/3+n^2R_{S2}/2,\ L'_2=L_\sigma/3+n^2L_{S2}/2,\ \overrightarrow{E'_{ac2}}=n\overrightarrow{E_{ac2}}e^{-j30^\circ} \quad (1)$$

where $n=V_{dc1}/V_{dc2}$ is the transformer ratio, R_{tr} and L_σ are the transformer resistance and leakage inductances (both referred to E_{ac1} side), L_{si}, R_{si} are arm inductors, and $\overrightarrow{E_{aci}}$ (i=1,2) are the AC voltage phasors of MMC1 and MMC2 respectively.

B. DC/DC Steady-State Equations

This section develops DC/DC model, based on Figure 2 which will be used for developing control strategy. The maximum rms value of phase-neutral MMC AC voltage is:

$$E_{acm1}=\frac{V_{dc1}}{2\sqrt{2}};\quad E_{acm2}=\frac{V_{dc2}}{2\sqrt{2}} \quad (2)$$

The phasors of ac voltage $\overrightarrow{E_{ac1}}$, $\overrightarrow{E'_{ac2}}$ are introduced as:

$$\overrightarrow{E_{ac1}}=E_{acd1}+jE_{acq1}=E_{acm1}M_{d1}+jE_{acm1}M_{q1} \quad (3)$$

$$\overrightarrow{E'_{ac2}}=E'_{acd2}+jE'_{acq2}=nE_{acm2}M_{d2}+jnE_{acm2}M_{q2} \quad (4)$$

and the control indices are defined as:

$$M_1=\sqrt{M_{d1}^2+M_{q1}^2};\quad M_2=\sqrt{M_{d2}^2+M_{q2}^2} \quad (5)$$

where subscripts *d* and *q* denote the corresponding phasor components in the rotating *dq* frame.

The current $\overrightarrow{I_{ac}}$ can be expressed as:

$$\overrightarrow{I_{ac}}=I_d+jI_q=\frac{\overrightarrow{E_{ac1}}-\overrightarrow{E'_{ac2}}}{R_E+jX_E} \quad (6)$$

where $X_E=2\pi fL_E;\ L_E=L_{ac}+L_{S1}/2+L'_2,\ R_E=R_{ac}+R_{S1}/2+R'_2$, f is the fundamental frequency of inner AC circuit. Substitute (3), (4) in (6) and after simplification:

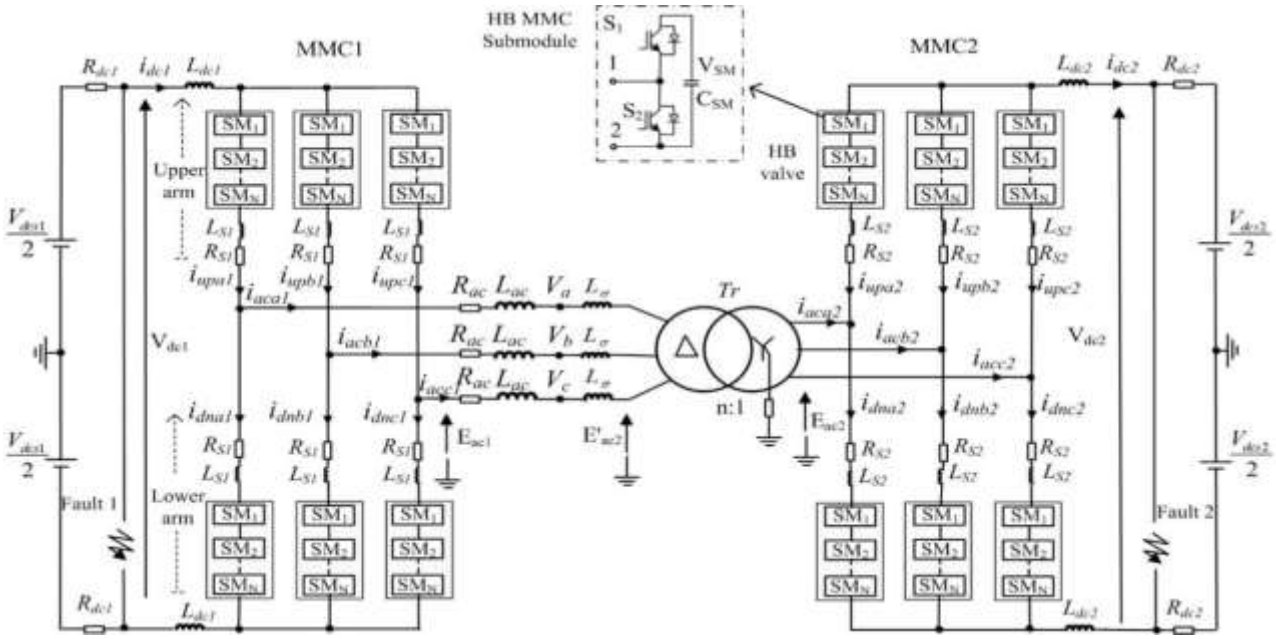

Figure 1 The MMC-based, DAB, isolated DC/DC converter for DC transmission grids.

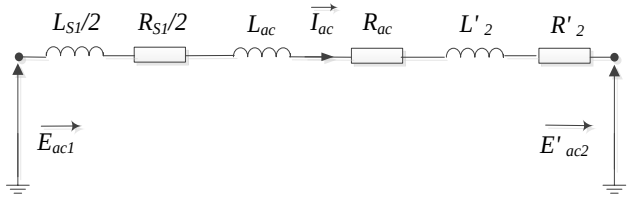

Figure 2 The equivalent per-phase AC circuit of DC/DC converter

$$I_d = \frac{R_E(E_{acd1}-E'_{acd2})+X_E(E_{acq1}-E'_{acq2})}{{R_E}^2+X_E^2} \quad (7)$$

$$I_q = \frac{R_E(E_{acq1}-E'_{acq2})-X_E(E_{acd1}-E'_{acd2})}{{R_E}^2+X_E^2} \quad (8)$$

The apparent powers at MMC1 and MMC2 S_1, S_2 are:

$$S_1 = 3\overrightarrow{E_{ac1}}(\overrightarrow{I_{ac}})^*; \quad S_2 = 3\overrightarrow{E'_{ac2}}(\overrightarrow{I_{ac}})^* \quad (9)$$

Replacing(6) in (9) and separating into real and imaginary, the expressions for the active powers P_1, P_2 and reactive powers Q_1 and Q_2 can be obtained:

$$P_1 = 3(E_{acd1}I_d + E_{acq1}I_q); \; Q_1 = 3(E_{acq1}I_d - E_{acd1}I_q) \quad (10)$$

$$P_2 = 3\left(E'_{acd2}I_d + E'_{acq2}I_q\right); \; Q_2 = 3(E'_{acq2}I_d - E'_{acd2}I_q) \quad (11)$$

If currents are replaced from (7), (8) in (10), (11) the full expressions for powers are obtained as shown in Appendix A. Assuming R_{ac}=0, in (6) the current components are:

$$I_d = \frac{E_{acq1}-E'_{acq2}}{X_E} \quad (12)$$

$$I_q = \frac{E'_{acd2}-E_{acd1}}{X_E} \quad (13)$$

III. CONVERTER CONTROLLER

A. The Control Goals

The main goals of DC/DC controller are:

1. Power order tracking,
2. Minimal phase current magnitude (to reduce conduction loss),
3. Phase current limiting below rated values under all conditions including DC faults.

The above control goals are achieved by manipulating four control signals: M_{d1}, M_{q1}, M_{d2}, M_{q2}.

B. Minimizing Current Magnitude

To minimize current magnitude ${I_{ac}}^2={I_d}^2+{I_q}^2$, two further control goals are proposed: 1) Keep $I_q=0$ and 2) minimize I_d.

To ensure $I_q=0$, (coordinate frame aligned with current) from (13) it follows:

$$E'_{acd2} = E_{acd1}; \Longrightarrow M_{d2} = M_{d1} \quad (14)$$

To achieve minimization of I_d, assuming $I_q=0$ for a given power $P_1=P_2$, from (10) and (11) we should maximize each: E_{acd1} and E_{acd2}. However M_{d1} and M_{d2} cannot be directly fixed at maximum value since PWM control index magnitude must be limited $0 \le M \le 1$. M_{q1} and M_{q2} should be allowed to vary freely, to enable full power transfer range as it is seen in (12). Therefore both M_d and M_q have to be adjusted with loading considering (5). Also, M_d should be allowed to vary to enable current control in inner loops.

In order to maximize M_{d1} and M_{d2} considering (5), two further control objectives are developed: 1) maximize M_1 and M_2 and 2) minimize M_{q1} and M_{q2}. Theoretically largest magnitude of modulation indices (M_1 and M_2) is 1, but there is need for some margin for dynamic control. It is proposed to regulate modulation indices to *0.95* in steady-state:

$$M_1 = 0.95; \; M_2 = 0.95; \quad (15)$$

Considering (5), (14) and (15), we can also conclude:

$$M_{q1} = -M_{q2} \quad (16)$$

The requirement to minimize M_{q1} and M_{q2} and considering a given d-current in (12) implies that lower X_E will give lower losses.

Equations (14),(15) or (15),(16) constitute fundamental control strategy for DAB MMC DC/DC to achieve minimal conduction losses and a defined operating point at any power.

C. Inner Current Loops

With common *50Hz*-operated AC/DC converters it is normal practice to regulate current components with control signals on the same axis (M_d controls I_d , M_q controls I_q) [1]. However with DC/DC converters, the fundamental frequency of inner circuit (*f*) is much higher, and therefore the speed-terms ($2\pi f L_E$) are much larger making decoupling more difficult. Equations (12) and (13) suggest cross-coupling for inner current control: M_d controls I_q while M_q controls I_d.

In DC/DC converters there is only one inner AC current, and it is essential that both MMCs, on each control channel, have current loops. In case of a DC fault on V_{dc1}, MMC2 sees fault on AC side and is able to reduce current, while in case of V_{dc2} fault it is MMC1 that can actively regulate current.

It is suggested that both MMC converters control the same AC current. Such approach can potentially lead to saturation of one of the controllers or control hunting (controllers acting against one another). This issue is avoided by employing active balancing according to (15), and (16). These conditions ensure that the two MMC equally participate in controlling the loading and that their control signals have the same margin from saturation.

D. Power Control

Equations (10) and (11), assuming $I_q=0$, show that I_d can be used to regulate active power. This implies that power regulator will generate d-current reference. Both MMC1 and MMC2 contribute to power control to ensure symmetry and back-up under all conditions.

E. Coordinate Frame Positioning

Figure 3 shows the phasor diagram considering the control strategy in (14)-(16).

The *dq* coordinate frame is therefore symmetrically positioned exactly between E_{ac1} and E'_{ac2}, and it is aligned with the current. The location of coordinate frame does not have a physically relevant AC bus since inductances L_{ac} and L_{σ} might be widely different. It is not required to use PLL (Phase Locked Loop) in the proposed control since control balancing in (15) and (16) will always ensure accurate coordinate frame positioning.

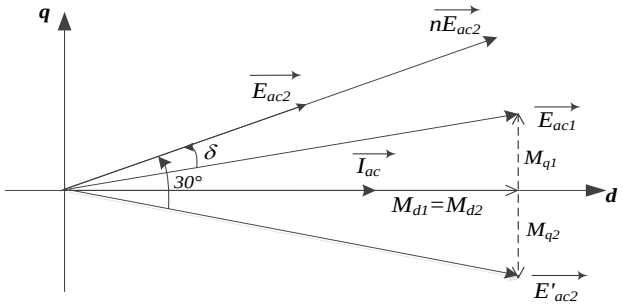

Figure 3 Vector diagram for AC variables and control

F. Steady-State Control Diagrams and Selection of X_E

Equation (21) in the Appendix A gives expressions for active power. Neglecting further resistance $R_{E,}$ and considering (16), introducing label: $M_q=M_{q1}=-M_{q2}$ the following power expression is obtained:

$$P_1 = \frac{6E_{acm1}^2 M_q \sqrt{0.95^2 - M_q^2}}{X_E} \quad (17)$$

Introducing the pu notation on the following base variables:

$$S_{base} = \frac{\left(\sqrt{3}E_{acm1}\right)^2}{Z_{base}} = \frac{3E_{acm1}^2}{Z_{base}};\ P_{pu}=P_1/P_{base},\ Z_{pu}=X_E/Z_{base}. \quad (18)$$

Power can be obtained in pu in DC/DC *dq* frame:

$$P_{pu} = \frac{2}{Z_{pu}} M_q \sqrt{0.95^2 - M_q^2} \quad (19)$$

Figure 4 illustrates the required M_q and power factor at MMC1 (or MMC2) for a range of X_{Epu}, at full power *P=1pu*. The test MMCs are designed in line with methods in [1] and [9], and parameters are listed in Appendix *B*. Smaller X_e is better because of higher power factor and lower current magnitude. However too small X_e will cause large transient current peaks for DC faults. Note that controller can regulate fault current magnitude but it has limited speed and the first current peak can be large if X_e is too small [1]. The PSCAD simulation with the test system recommended X_e.=*0.53pu*, which results in M_q=*0.3* at full power. In practice it is frequently simpler to design transformer and a series reactor when transformer with such large reactance is required.

Figure 5 shows the power variation for control signal M_q change, with the selected X_e. Also the powers measured on PSCAD are illustrated to confirm accuracy of the model.

G. Controller topology

Figure 6 shows the control diagram for both MMCs. K_{p1}-K_{p3}, K_{i1}-K_{i4} are proportional and integral gains of the PI controllers. The measured power is the average of the two MMC DC powers, which eliminates impact of power direction on control operation. A *350Hz* voltage controlled oscillator provides fixed sawtooth angle, which needs to be corrected at MMC2 to account for *30deg* Y/D phase shift.

The outer control structure consists of active power control, balancing and M_1, M_2 regulation. It is seen that both MMC control the same power. The balancing control loop compares M_q at the two bridges and using PI control acts on I_{dref}, but in opposite direction at the two bridges. The control rule in (15) is achieved using a PI controller which compares local modulation index magnitude with reference value of 0.95 and adjusts local I_q current reference.

The inner dq current loops are identical at the two MMCs (with different sign). Note that M_d is limited with priority on M_q to ensure fast active power control under all conditions.

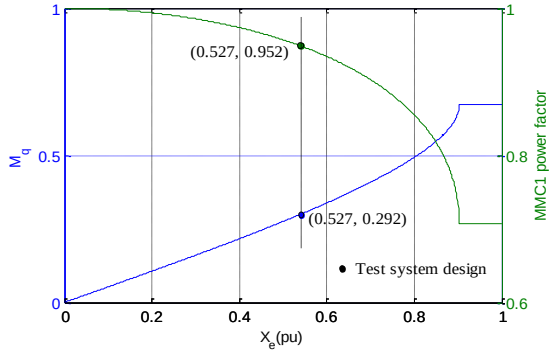

Figure 4 M_q and MMC1 power factor for full power versus X_e(pu)

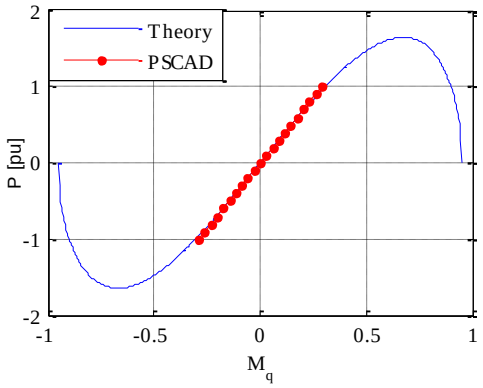

Figure 5 Active power versus M_q with X_E=*0.53pu*.

IV. SIMULATION RESULTS

A. MMC Converter Average Value Model

Each MMC consists of six arms and the number of inserted cells in each arm is the control output in Figure 6.

The number of inserted cells for phase *i*, N_u (u-upper and l-lower arm) is derived from the ABC frame fundamental control M_{fi} and the circulating current control M_{hi}:

$$N_{ui} = \frac{1+M_{fi}+M_{hi}}{2} \qquad N_{li} = \frac{1+M_{fi}-M_{hi}}{2} \tag{20}$$

Figure 7 shows the AVM (Average Value Model) for upper arm of phase a, which represents both normal operation and blocked state, where switch controls blocked/unblocked state and which is slightly simplified model from [17].

Each MMC is blocked when it's DC voltage is below *0.8pu*, or when arm current exceeds *2pu*. In blocked state the cell voltage is correctly represented since cell may be charged through diode D_a (but not through control).

The arm voltage calculation is shown in Figure 7(b) [1],[17], where C_{arm} is the equivalent arm capacitance, $C_{arm}=C_{SM}/N$, and N is the number of cells in an arm.

B. Normal Operation

Figure 8 shows the simulation results for power step at *1s* and power reversal at *1.15s*. Initially, *600MW* is delivered from MMC1 to MMC2, it is reduced to 0.1pu and then the power reference is changed to *-600MW*.

In Figure 8 (b) it is seen that magnitude of both control indices are well regulated at 0.95, while at low power M_d is increased as seen in Figure 8 c).

Figure 8 (c) and (d) show the dynamics of *d* and *q* axis control indices of two MMCs. The relation of M_{q1}=-M_{q2} is maintained at all powers, as well as balance M_{d1}=M_{d2}.

Figure 8 (e) show the dynamics of the current $\overrightarrow{I_{ac1}}$. Fast and accurate tracking of reference currents by the inner *dq* current controller is observed. Figure 8 (f) confirms that current magnitude is low at low power.

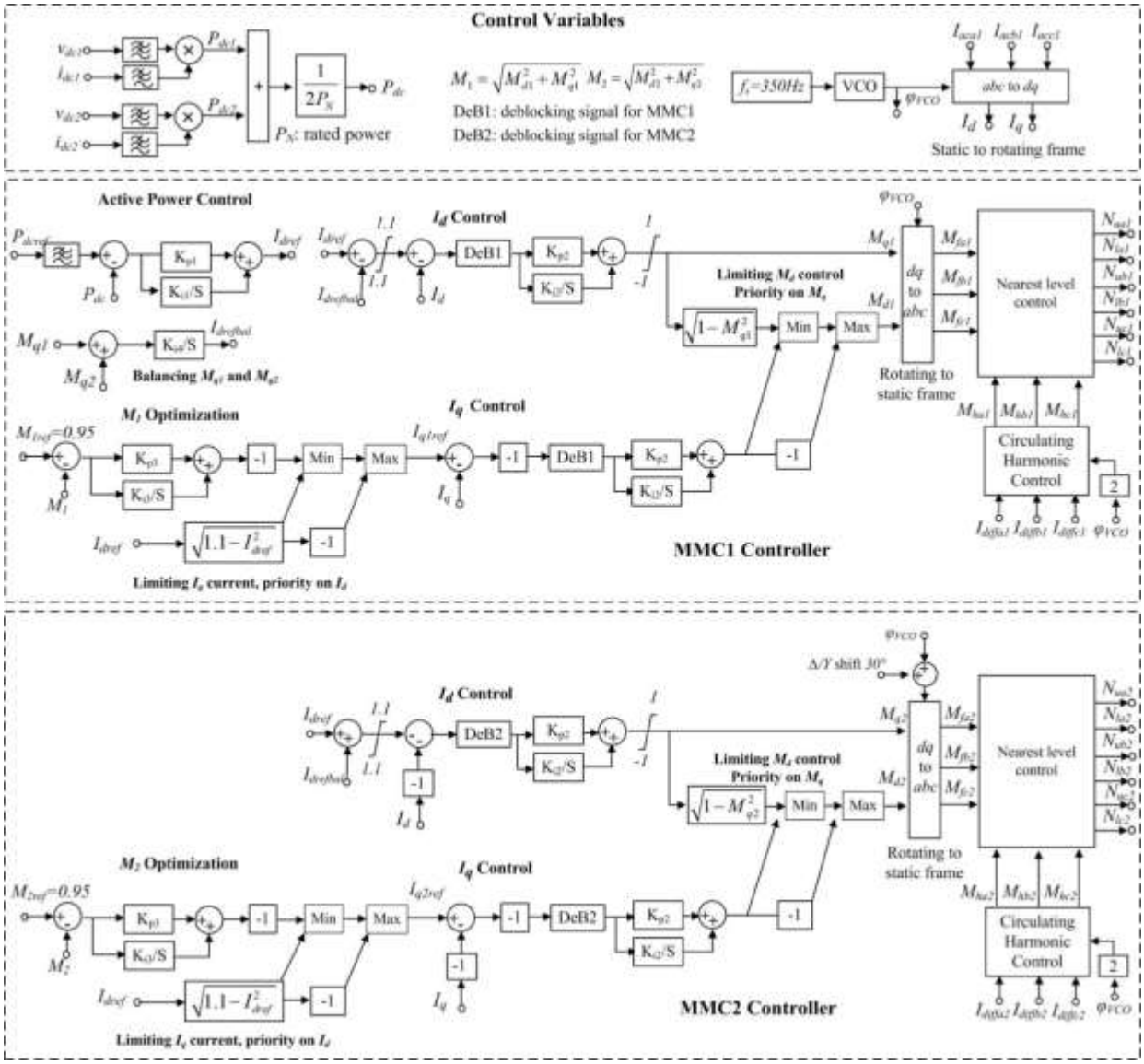

Figure 6 DC/DC converter controller

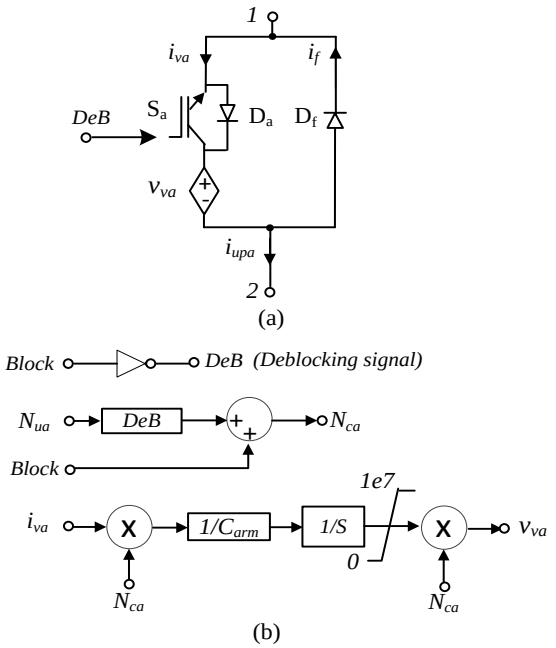

Figure 7 Average value ABC frame MMC model for upper arm of phase *a*

C. DC Faults

Two worst-case zero-impedance DC faults are tested, on each DC bus as shown in Figure 1. Fault 1 occurs at V_{dc1} at *0.5s* and fault 2 occurs at V_{dc2} at *1.0s* while converter is operating at full power and each fault lasts *0.2s*.

Figure 9 (a) shows the DC voltages and Figure 9 (b) shows the status of active power. It is observed the DC/DC recovers full power in about *0.1s* after each fault.

Figure 9 (c) shows the modulation indices during this test. When fault 1 occurs at MMC1 side, the modulation index M_2 reduces in order to reduce fault current, while when fault 2 occurs, the modulation index M_1 enables phase current control. There is no saturation and contribution of two MMC is balanced in all operating conditions.

Figure 9 (d) shows the *d* and *q* components of the current at E_{ac1} side of the transformer. During fault conditions, both current components are regulated at saturation values for current reference signals which are *1.1pu*. After the faults, the *dq* currents are recovered to their references within *0.1s*.

Figure 9 (e) and (f) show in ABC frame the AC voltage and current at E_{ac1} side of the transformer. The drop of control index significantly reduces the AC voltages during the DC faults. The AC voltage is not identical for the two faults because inductances L_{ac} and L_σ are different. The peak AC currents are restricted below 2*pu* under all conditions.

Figure 9 (g) and (h) show the arm currents of MMC1 and MMC2 which are important for semiconductor dimensioning. For a blocked MMC, peak arm currents are large because of cell capacitor discharge and this causes MMC blocking. In steady-state AC component of arm current is larger than for controlled MMC because of diode bridge operation. The controlled MMC bridge has well regulated arm currents with minimal DC offset indicating low power transfer.

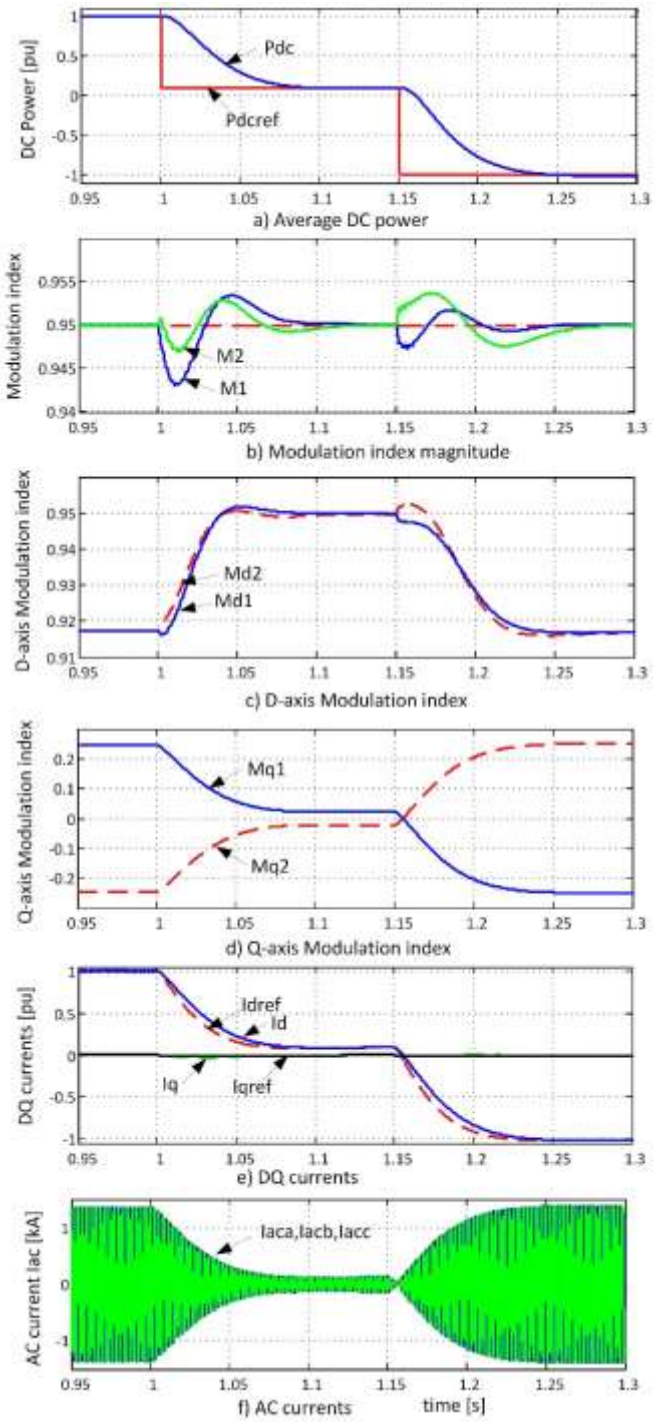

Figure 8 Power step from 1pu to 0.1pu at 1s, and then to -1pu at 1.15s.

When a DC fault occurs and when it is cleared, arm currents may develop transient peaks due to the discharging/charging of cell capacitors. These peaks are lower than rated peak values and can be reduced further by increasing inductor L_{ac}.

Figure 9 (i) and (j) illustrate the cell capacitor voltages of MMC1 and MMC2. When an MMC is exposed to DC fault it is blocked to prevent large IGBT currents from cell discharge. This blocking is necessary even though the AC

infeed current is small. In blocked state cell capacitor voltages are constant, since all the currents flow through anti-parallel diodes without affecting the capacitors. The MMC is de-blocked when DC voltage recovers.

The cell voltage shows *30%* peaks for DC faults, which is acceptable for most extreme dc faults. Cell capacitance is designed according to the methods given in [9].

Therefore in the proposed control strategy, only fault-facing MMC is blocked for low DC voltage, and when DC voltage recovers the DC/DC establishes normal power flow.

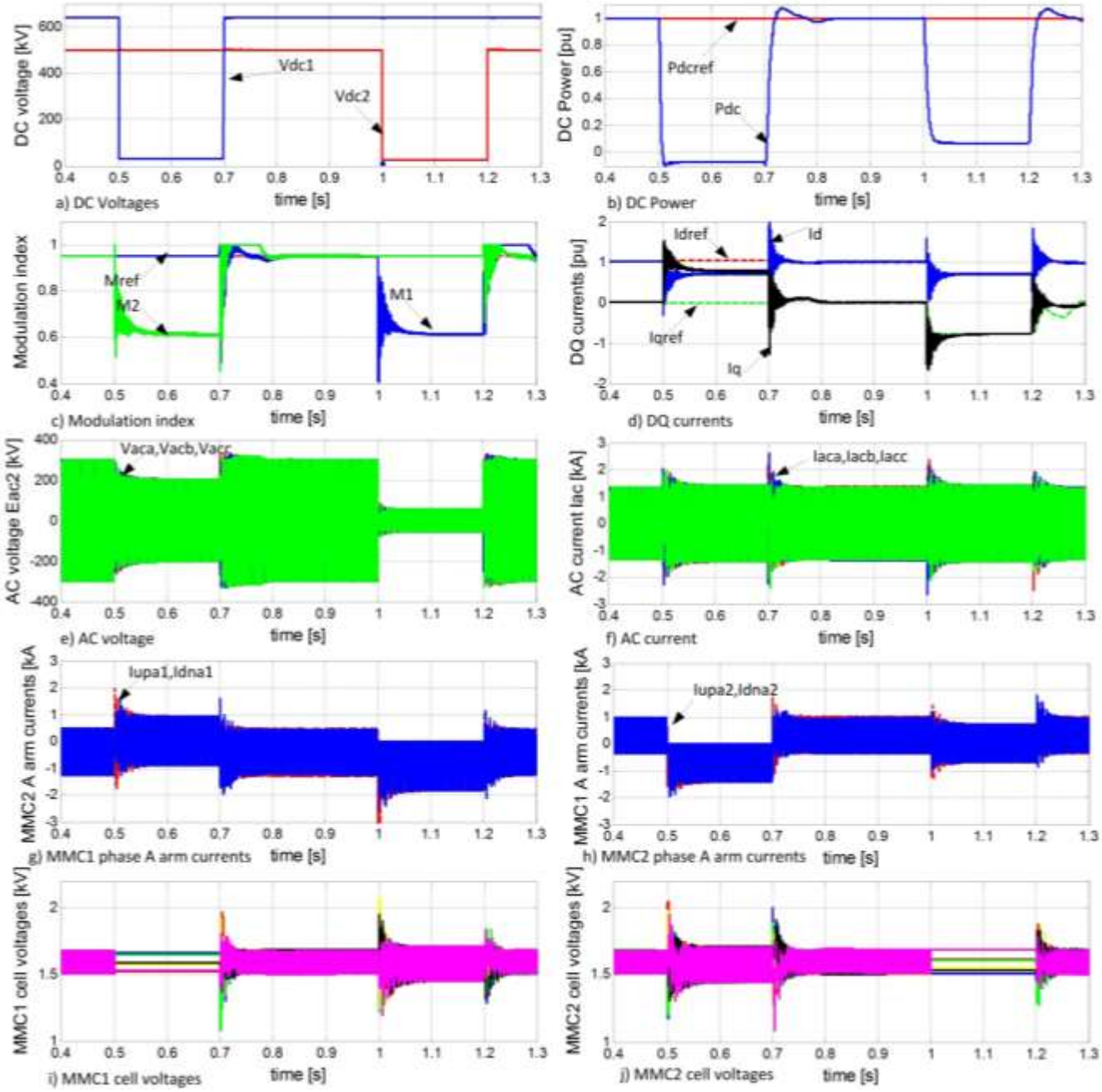

Figure 9 DC/DC converter response for *0.2s* transient DC fault on V_{dc1} at *0.5s*, and on V_{dc2} at *1s*.

V. CONCLUSION

By analyzing *dq* frame model of DAB MMC DC/DC converter the paper firstly derives control strategy to enable minimal current at any power level. This is achieved if modulation index magnitude is controlled in feedback manner at maximal possible value. It is concluded that power can be regulated using M_q control on both MMC bridges. It is also essential to maintain balance between the two bridges which is achieved when q-control signals are equal in magnitude.

The DC fault study concludes that it is possible to control current for a fault at either DC bus, and that two MMC may utilize the same current feedback signal. The essential aspect

of the proposed controller is that each MMC employs two inner current control loops in all operating modes.

The PSCAD simulation concludes that the DAB MMC DC/DC operation is satisfactory for power steps and fast power reversal. Extreme DC faults on both dc busses are also simulated and excellent controller responses are observed. The currents are well controlled during *200ms* DC faults and peak current magnitudes are below *2pu* enabling DC/DC continued operation through worst dc faults.

VI. REFERENCES

[1] D. Jovcic and K. Ahmed, *High-Voltage Direct Current Transmission: Converters Systems and DC Grids*, Wiley 2015.

[2] T K Vrana, Y Yang, D Jovcic, S Dennetière, J Jardini, H Saad, 'The CIGRE B4 DC Grid Test System," ELECTRA issue 270, October 2013, pp 10-19.

[3] CIGRE WG B4.52 "Feasibility of HVDC grids," CIGRE technical brochure 533, Paris, April 2013

[4] Abdelrahman Abbas Hagar and Peter W. Lehn "Comparative evaluation of a new family of transformerless modular DC–DC converters for high-power applications," IEEE Transactions on Power Delivery, vol. 29, no. 1, Feb.2014, pp.444-452.

[5] H. Yang, J. Qin, S. Debnath and M. Saeedifard, "Phasor domain steady-state modelling and design of the DC-DC modular multilevel converter," IEEE Transactions on Power Delivery, vol. PP, no. 99, 2016, early access DOI 10.1109/TPWRD.2016.2515498.

[6] D. Jovcic and L. Zhang, "LCL DCDC converter for DC grids," *IEEE Transactions on Power Delivery*, vol. 28, no. 4, Oct. 2013, pp. 2071-79.

[7] C.D. Barker, C.C. Davidson, D.R. Trainer, R.S. Whitehouse "Requirements of DC-DC converters to facilitate large DC grids," CIGRE Paris 2012, paper B4-204.

[8] T. Luth, M.M.C. Merlin, T.C. Green, F. Hassan, and C.D. Barker, "High-frequency operation of a DC/AC/DC system for HVDC applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, Aug. 2014, pp. 4107-15.

[9] A. Jamshidifar, M. Hajian, D.Jovcic and Y Audachya, "High power MMC VSC optimal design for DC/DC converter applications," *IET Power Electronics*, vol. 9, iss. 2, Feb. 2016, pp 247-255.

[10] Z. Xing, X. Ruan, H. You, X. Yang, D. Yao, and C. Yuan, "Soft-switching operation of isolated modular DC/DC converters for application in HVDC grids," *IEEE Transaction on Power Electronics*, vol. 31, no. 4, pp. 2753-2766, 2016.

[11] C. Sun, J. Zhang, X. Cai, and G. Shi, "Voltage balancing control of isolated modular multilevel dc-dc converter for use in dc grids with zero voltage switching," *IET Power Electronics*, vol. 9, iss. 2, pp. 270-280, Feb. 2016

[12] Y. Chen, Y. Cui, X. Wang, X. Wei, and Y. Kang, "Design and implementation of the low computational burden phase shifted modulation for DC-DC modular multilevel converter," *IET Power Electronics*, vol. 9, iss. 2, pp. 256-269, 2016.

[13] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y. R. Novaes, "Isolated DC/DC structure based on modular multilevel converter," *IEEE Transactions on Power Elect.* vol. 30, no. 1, Jan. 2015, pp. 89-98.

[14] Asier Garcia-Bediaga; Irma Villar; Alejandro Rujas; Ion Etxeberria-Otadui; Alfred Rufer "Analytical Models of Multiphase Isolated Medium-Frequency dc-dc Converters" *IEEE Transactions on Power Electronics*, early access DOI: 10.1109/TPEL.2016.2570941, 2016,

[15] B. Zhao, Q. Song, J. Li, Y. Wang, and W. Liu, "High-Frequency-Link modulation methodology of DC-DC transformer based on modular multilevel converter for HVDC application: comprehensive analysis and experimental verification," *IEEE Transactions on Power Electronics*, vol. PP, pp. 1-1, 2016.

[16] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday, and B. W. Williams, "Quasi Two-Level Operation of Modular Multilevel Converter for Use in a High-Power DC Transformer With DC Fault Isolation Capability," *IEEE Transactions on Power Electronics*, vol. 30, pp. 108-123, 2015.

[17] F. B. Ajaei and R. Iravani, "Enhanced equivalent model of the modular multilevel converter*," IEEE Transactions on Power Delivery*, vol. 30, no. 2, Apr. 2015, pp. 666-673

VII. APPENDIX

A. Active and Reactive Powers at MMC1 and MMC2

Using the model defined in (1)-(11), the active and reactive powers can be expressed:

$$P_1 = 3 \times \left(\frac{R_E\left(E_{acd1}^2+E_{acq1}^2-E_{acd1}E'_{acd2}-E_{acq1}E'_{acq2}\right)}{{R_E}^2+X_E^2} - \frac{X_E\left(E_{acd1}E'_{acq2}-E_{acq1}E'_{acd2}\right)}{{R_E}^2+X_E^2}\right)$$

$$Q_1 = 3 \times \left(\frac{X_E\left(E_{acd1}^2+E_{acq1}^2-E_{acq1}E'_{acq2}-E_{acd1}E'_{acd2}\right)}{{R_E}^2+X_E^2} + \frac{R_E\left(E_{acd1}E'_{acq2}-E_{acq1}E'_{acd2}\right)}{{R_E}^2+X_E^2}\right)$$

$$P_2 = 3 \times \left(\frac{R_E\left(E_{acd1}E'_{acd2}+E_{acq1}E'_{acq2}-{E'_{acd2}}^2-{E'_{acq2}}^2\right)}{{R_E}^2+X_E^2} - \frac{X_E\left(E_{acq1}E'_{acd2}-E_{acd1}E'_{acq2}\right)}{{R_E}^2+X_E^2}\right)$$

$$Q_2 = 3 \times \left(\frac{X_E\left(E_{acq1}E'_{acq2}+E_{acd1}E'_{acd2}-{E'_{acd2}}^2-{E'_{acq2}}^2\right)}{{R_E}^2+X_E^2} + \frac{R_E\left(E_{acd1}E'_{acq2}-E_{acq1}E'_{acd2}\right)}{{R_E}^2+X_E^2}\right) \quad (21)$$

B. Test System Parameters

TABLE I TEST SYSTEM PARAMETERS

Items	**Value**	**Items**	**Value**
Active power P	600MW	Fundamental frequency f	350 Hz
DC bus voltage V_{dcs1}	±320kV	DC bus voltage V_{dcs2}	±250 kV
DC resistance R_{dc1}	0.5 Ω	DC resistance R_{dc2}	0.5 Ω
DC inductance L_{dc1}	3mH	DC inductance L_{dc2}	3mH
Transformer turn ratio n	1.28	Transformer leakage inductance L_σ	0.16 mH
Series inductance L_{ac}	50mH	AC total resistance R_{ac}	0.08 Ω

Items	**MMC1 value (i=1)**	**MMC2 value (i=2)**
Number of SMs per arm	400	313
SM capacitance C_{SM}	1.25mF	1.6mF
Arm inductance L_{si}	13.73mH	8.37mH
Arm resistance R_i	0.51 Ω	0.25 Ω
SM capacitor voltage V_{SM}	1.6kV	1.6kV
IGBT	5SNA1200G450300	5SNA1200G450300

VIII. BIOGRAPHIES

Dragan Jovcic (SM'06, M'00, S'97) obtained a Diploma Engineer degree in Control Engineering from the University of Belgrade, Serbia in 1993 and a Ph.D. degree in Electrical Engineering from the University of Auckland, New Zealand in 1999. He is currently a professor with the University of Aberdeen, UK where he has been since 2004. In 2008 he held visiting professor post at McGill University, Montreal, Canada. His research interests lie in the HVDC, FACTS, DC grids and control systems.

Huibin Zhang received M.Sc. degree (with Distinction) in Heriot-Watt University in 2004, and the award of PhD in University of Strathclyde in 2009. From 2008 to 2011 he worked as a research fellow in University of Strathclyde. Currently he is a research assistant with University of Aberdeen. His research interests include DC/DC converters, active power filters, and renewable energy system.